REMARKS

I. Present Disposition of the Claims

The Applicants wish to reiterate thanks to the Examiner for the useful comments in the non-final Office Action mailed June 2, 2003. In addition, the Applicants reiterate thanks for the useful comments from the telephone interview during the June 11, 2003, which have been herein incorporated. The present invention related to integrated circuit semiconductor circuits and anti-reflective coating fabrication techniques used in dual gate semiconductor technology, such as FLASH memory technology. More particularly, the present invention related to integrated semiconductor circuits and fabrication techniques for forming sidewall structure on the sidewalls of the transistor gates used in dual gate semiconductor technology, such as FLASH memory technology. The Summary of the Invention paragraph has been herein amended, without prejudice, and independent Claims 14,17, 19, and 21, and dependent Claims 15 and 18 have been herein amended, without prejudice, to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that the claims were allowable as originally filed.

Specifically, based on the June 11 telephonic interview with the Examiner, the Specification on page 2, line 21, on page 4, line 18, and on page 5, lines 4-5 have been herein amended to replacing silicon germanium(SiGe) with <u>insulator silicon germanium (SiGe)</u> to clarify that the claimed structure includes high resistivity SiGe and not conducting SiGe. No new matter was introduced during this Amendment to the Specification. Further, independent Claim 14 and dependent Claims 15 and 18 have been herein amended replacing SiGe with <u>insulator SiGe</u> to clarify the spacer is non-conductive, independent Claims 17, 19, and 21 have been herein amended by deleting the core memory stack limitation a semiconductor material; and a dielectric material defining respective sidewall portions and replacing this limitation with "<u>a first polysilicon layer, a dielectric layer over the first polysilicon layer, and a second polysilicon layer over the dielectric layer</u>" which is fully supported by the Specification, p. 4, ll. 1-5. Therefore, reconsideration of the present application in light of the foregoing proposed amendment and these remarks is respectfully requested.

II. Rejection of Claims 14-16, 18 and 21 under 35 U.S.C. § 112, first paragraph:

Claims 14-16, 18 and 21 have been rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. The Office Action states:

> The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The limitation "spacer structure comprises .....SiGe" in claims made claims un-enabled because it is known in the art SiGe is a conductive material and the spacer being formed of SiGe would electrically connect[] the silicon layers ([P1]) and (P2) together, so the memory device does not work.

Notwithstanding independent Claims 14, 17, 19, and 21 having been herein amended, as discussed supra, and dependent Claims 15, 16, 18 and 20 now subsuming the limitations respectively of the independent claims from which they depend, the Applicants respectfully hereby traverse these grounds for rejection.

As shown in Exhibit A, the definition of an insulator is a high resistance material. Exhibit B shows a non-limiting example for the present invention that SiGe is an insulator. In this non-limiting example, the intrinsic resistance of SiGe is about .575 X 10^5 ohms/cm so SiGe qualifies as an insulator. It should it be noted, however, that insulator SiGe can have various resistance values other than the non-limiting example shown above. Therefore, Insulator SiGe will not conduct electricity from silicon layer P1 to silicon layer P2. As such, the Applicants have herein amended the Specification to include the sidewall spacer SiGe is an insulator and is not a conductive material. Therefore, the Applicants respectfully request that these grounds for rejection be withdrawn and the Claims 14-16, 18 and 21 pass to allowance.

III. Rejection of Claims 17-21 under 35 U.S.C. § 103(a):

Claims have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Taniguchi (US 6,559,494) ("Taniguchi")in view of Cho et al. (US 6,027,971) ("Cho"), stating:

> Taniguchi discloses a semiconductor memory device comprising: a silicon substrate (1) including a periphery memory region (A) and a core memory region (B); a transistor formed on the peripheral memory region; one set of dual gate core memory structures formed in the core memory region, the dual gate core memory structures including a stacked layer arrangement of semiconductor layer (6) and a dielectric material layer (9) defining respective sidewall; sidewall spacer structures (11) of silicon nitride having a thickness of 800 angstroms (Taniguchi's col. 7 lines 59-61) formed on the sidewall portions of dual gate core memory structures; a coating residing also formed of silicon nitride layer (11) on the

periphery memory region to provide a pattern (the gate stack of the transistor) on the periphery memory region. See Taniguchi Fig. 20.

Taniguchi does not explicitly teach that the silicon nitride for formed spacer structures (21) have a chemical formula Si_3N_4.

Notwithstanding independent Claims 17, 19, and 21 having been herein amended, as discussed supra, and dependent Claims 18 and 20 now subsuming the limitations of independent Claims 17 and 19 respectively from which they depend, the Applicants respectfully hereby traverse these grounds for rejection.

Contrary to the present invention, Taniguchi teaches a memory stack comprising "a polyside layer 8 [that] is anisotropically etched through the mask of the patterned oxide film 9 to form gate electrodes having a gate length of approximately 0.3 um" (Col. 7, ll. 42-45; Exhibit C). The **polyside layer 8** is composed of "a **phosphorous doped polysilicon film 6,** wherein the phosphorous is doped at a concentration of 5 x 10^{20} atoms/cm^3 **and tungsten silicide film (WSi2) 7** are respectively deposited with a thickness of approximately 500 Angstroms by CVD, thereby forming a so-called **polyside double-layered film 8** (first conductive film)(which may be sometimes herein referred to simply as a polyside)" (Col. 7, ll. 27-34). Further, Taniguchi teaches "a silicon nitride film 11 is deposited with a thickness of approximately 800 angstroms by CVD. The **silicon nitride film 11 serves as sidewalls of the MOS transistor** having a LDD structure" Col. 7, ll. 59-63; Exhibit C). In addition, Taniguchi teaches "an approximately 1000 Angstrom thick silicon oxide film 9 deposited by CVD as shown" (Col. 7, ll. 32-37, Exhibit C). In other words, Taniguchi teaches **memory cell stack structure comprising a polyside 8, a thick silicon oxide film 9, and a silicon nitride layer 11.**

In contrast to Taniguchi, the presently claimed core memory stack structure included in herein amended Claims 17, 19, and 21 comprises "**a first polysilicon layer, a dielectric layer over the first polysilicon layer, and a second polysilicon layer over the dielectric layer**" (Exhibit D). Polysilicon (Poly Si) is commonly used as a gate contact in silicon MOS devices transistors (Exhibit E). Further, Taniguchi teaches a two layer polysilicon, i.e. a **phosphorous doped polysilicon film 6** and **tungsten silicide film (WSi2) 7 protected by a SiN** layer 11, while in contrast the present invention structure has two layers of polysilicon separated by a dielectric layer and **this stack is not protected by a SiN layer.** Further, Tanguichi has SiN sidewalls and so does the present invention; however, for the present

invention SiN is not covering the second polysilicon layer which is structurally different than Taniguchi (Exhibit C, D). Thus, independent Claims 17, 19 and 21 of the present invention are not taught, suggested, nor motivated by Taniguchi.

Contrary to the present invention, Cho teaches a core memory stack structure comprising a first gate insulating material 54, a conductive layer 56, an insulator layer 58, a conductive layer 60, and a protective covering with a Si_3N_4 layer 64 that covers both the conductive layer 60 and provides a sidewall layer of the core memory stack structure (Exhibit F). In contrast to Cho core memory stack structure, the present **invention core memory structure does not include a Si_3N_4 layer 64 that covers a second polysilicon layer top portion** and only covers the sidewalls (Exhibit D). Further, Cho teaches against removal of the Si_3N_4 on top of conductive layer 60 because the Cho core memory cell requires protection during impurity implantation (Exhibit G). Consequently, Taniguchi even in view of Cho, teaches against removal of a SiN layer on top of the structure. Thus, the claimed invention incorporating "**a first polysilicon layer, a dielectric layer** over the first polysilicon layer, and **a second polysilicon layer** over the dielectric layer" with the limitation "**a sidewall spacer structure** comprising an **anti-reflective coating material** for protecting said core memory stacks during etching operation" is not taught, suggested, nor motivated by Taniguchi, even in view of Cho.

Moreover, the Manual for Patent Examiners' Practice paragraph 2142 addresses the 103(a) basis for rejection, mandating that ". . . To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991), MPEP Section 706.02(j). "Mere fact that prior art may be modified to reflect features of claimed invention does not make modification, and hence claimed invention, obvious unless desirability of such modification is suggested by prior art . . .", *In re Fritch*, 922 F.2d 1260, 23 USPQ.2d 1780, at p. 1780 (Fed. Cir. 1992).

Moreover, where each reference fails to state each and every element of the claimed invention or provide a rationale to modify the elements present, reliance upon a broad statement of 'obvious design' is not an appropriate basis of rejection under 35 U.S.C. 103(a). According to *In re Gal*, 25 USPQ2d 1076 at 1079, "The Commissioner does not explain why or how Matsumura, or the general knowledge of the art, provides a teaching, suggestion, or motivation to modify the Matsumura chip structure in order to produce the Gal chip structure." Note that *Gal* has been characterized as stating that a "finding of 'obvious design choice' precluded where the claimed structure and the function it performs are different from the prior art." *In re Chu*, 36 USPQ2d 1089 at 1095. This view is supported by *In re Lee*, rejection of claims based upon an assumption of 'obvious design' cannot stand. *In re Lee* states that:

> This court explained in *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697, that "deficiencies of the cited references **cannot be remedied by the Board's general conclusions** about what is ` **basic knowledge' or `common sense.'**" The Board's findings must extend to all material facts and must be documented on the record, lest the "haze of so-called expertise" acquire insulation from accountability. "**Common knowledge and common sense,**" even if assumed to derive from the agency's expertise, **do not substitute for authority when the law requires authority** . *See Allentown Mack*, 522 U.S. at 376 ("Because reasoned decision making demands it, and because the systemic consequences of any other approach are unacceptable, the Board must be required to apply in fact the clearly understood legal standards that it enunciates in principle ....") In re Lee, 61 USPQ2d 1430, 1434 (CA FC 2002).

As such, the Office Action stating, "Taniguchi does not explicitly teach that the silicon nitride forming spacer structures (21) have the chemical formula Si_3N_4" without stating any other reasoning than "[i]t is known in the art and also taught in Cho that silicon nitride is usually preferred to Si_3N_4 in semiconductor device[s]. Therefore, it would have been obvious to one of ordinary skill in the art to form sidewall spacer structures of silicon nitride (Si_3N_4) as taught by Cho et al." does not satisfy the requirement of a 103(a) rejection. Stated differently, "**Common knowledge and common sense,**" even if assumed to derive from the agency's expertise, **do not substitute for authority when the law requires authority.** Furthermore, **"a retrospective view of inherency** is **not a substitute** for **some teaching or suggestion which supports the selection** and use of various elements in the particular claimed combination." *In re Newell*, 13 U.S.P.Q. 1248 at 1250. As such, the references cited to reject the Applicants claims do not in fact provide an adequate basis for rejection under 35 U.S.C. § 103(a), the Applicants respectfully request these rejections be withdrawn.

Moreover, even if you combine the Taniguchi structure with the Cho sidewalls, the **combination would be inoperable** because **Taniguchi teaches that "holes are made in the oxide films 14** at portions above the source/drain regions 10a and in between adjacent electrodes 8 of the memory cell portion A (col. 8, ll. 37-40)" whereas **the cited art Cho teaches an insulator sidewall spacer covering the holes of the Taniguchi structure**. Thus, the combination of Taniguchi with Cho would be inoperable.

Thus, Taniguchi, even in view of Cho, does not teach, suggest, nor motivate herein amended independent Claims 17, 19, and 21 reciting:

17. **(currently amended)** A semiconductor memory device, comprising:
    a. a silicon substrate;
    b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;
    c. a core memory region also delineated on said substrate,
    said core memory region having at least one set of dual gate core memory structures thereon formed,
    said dual gate core memory structures comprising at least one pair of spaced core memory stacks,
    and
    said core memory stacks comprising:
    a first polysilicon layer,
    a dielectric layer over the first polysilicon layer, and
    a second polysilicon layer over the dielectric layer;
    d. a sidewall spacer structure comprising a anti-reflective coating material for protecting said core memory stacks during etching operations, wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and ≺1000 Å); and
    e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

19. **(currently amended)** A semiconductor memory device, comprising:
    a. a silicon substrate;
    b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;
    c. a core memory region also delineated on said substrate,
    said core memory region having at least one set of dual gate core memory structures thereon formed,
    said dual gate core memory structures comprising at least one pair of spaced core memory stacks,
    and
    said core memory stacks comprising:
    a first polysilicon layer,
    a dielectric layer over the first polysilicon layer, and
    a second polysilicon layer over the dielectric layer;

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations,
wherein said anti-reflective coating material comprises **insulator** silicon germanium (SiGe) being compatible with ion implantation and salicidation fabrication processes, and
wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

21. **(currently amended)** A semiconductor memory device, comprising:

a. a silicon substrate;

b. a periphery memory region delineated on said substrate, said periphery memory region having at least one periphery memory element thereon formed;

c. a core memory region also delineated on said substrate,
said core memory region having at least one set of dual gate core memory structures thereon formed,
said dual gate core memory structures comprising at least one pair of spaced core memory stacks,
and
said core memory stacks comprising:
a first polysilicon layer,
a dielectric layer over the first polysilicon layer, and
a second polysilicon layer over the dielectric layer;

d. a sidewall spacer structure comprising an anti-reflective coating material for protecting said core memory stacks during etching operations,
wherein said anti-reflective coating material comprises a material selected from a group consisting of silicon oxynitride (SiON), silicon nitride (Si_3N_4), and **insulator** silicon germanium (SiGe), said group being compatible with ion implantation and salicidation fabrication processes, and
wherein said anti-reflective coating material comprises a thickness ranging from 300 Å up to 1000 Å (i.e., ≥300 Å and <1000 Å); and

e. a coating residing on said periphery memory region comprising said anti-reflective coating material, wherein said coating is adapted to protect said periphery memory region during etching operations and to provide a pattern for said at least one periphery memory element on said periphery memory region.

As such, Taniguchi, even in view of Cho, does not teach the herein amended independent Claims 17, 19, 21 nor the dependent Claims 18 and 20 now respectively subsuming the limitations of herein amended independent claims from which they depend. Therefore, the Applicants respectfully request that these grounds for rejection be withdrawn and Claims 17-21 pass to allowance.

III. Rejection of Claims 1, 4, 14, 17, 19, and 21 as being Expressions of Dual Purpose and Being Used for Lithographic Patterning:

Claims 1, 4, 14, 17, 19, and 21 have been rejected as expressions of "dual purpose" and "being used for lithographic patterning for protecting said stacked layer arrangement during the etching operations." First, Claims 1 and 4 have been previously canceled; thus, rendering moot these grounds for rejection. Second, Claims 14, 17, 19 and 21 do not claim any limitations such as "dual purpose" or "being used for lithographic patterning for protecting said stacked layer arrangement during the etching operations." Thus, Applicants respectfully believe that these grounds are moot and respectfully request that these grounds of rejection be withdrawn and Claims 14, 17, 19 and 21 pass to allowance.

CONCLUSION

Accordingly, the Specification, and the independent Claims 14, 17, 19 and 21 dependent Claims 15 and 18 have been herein amended to better encompass the full scope and breadth of the present invention, notwithstanding the Applicants' belief that application would have been allowable as originally filed. The proposed amendment to the Specification and the Claims are believed to be fully supported by the originally filed Specification. For all the above advanced reasons, the Applicants respectfully submit the application is in condition for allowance. Therefore, favorable consideration of the foregoing proposed amendment and remarks is kindly requested. ***The Examiner is further cordially invited to telephone the undersigned for any reason which would advance the pending claims to allowance.***

Respectfully submitted,

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EXHIBIT A

(Definition for "Insulator")

Semiconductor Glossary

Semiconductor OneSource

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Term (Index)	Definition
insulator	very high resistivity material used to electrically separate conducting materials.

glossary semiconductor circuit board eeprom eprom prom layout silicon glossary description definition knowsemiconductors education knowledge board

EXHIBIT A

EXHIBIT B

(Silicon Germanium Intrinsic Resistivity)
2 pages

The General Properties of Si, Ge, SiGe, SiO_2 and Si_3N_4

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June 2002

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A. Introduction

This paper summarizes basic physical properties of Si, Ge, SiGe, SiO_2 and Si_3N_4. It also list several physical constants and conversion factors. The information is presented in table format with explanations of any approximations or equations used.

B. The Basic Properties of Si, Ge, and SiGe

The following table summarizes many of the basic physical properties of Silicon, Germanium, and Silicon Germanium at different concentrations. The concentrations are given in the form of $Si_{1-x}Ge_x$ where x represents the percent composition of Germanium.

Properties	Ge	$Si_{.25}Ge_{.75}$	$Si_{.5}Ge_{.5}$	$Si_{.75}Ge_{.25}$	Si
Atoms/cm^3	4.42×10^{22} Ge	$*4.415 \times 10^{22}$	$*4.61 \times 10^{22}$	$*4.805 \times 10^{22}$	5.0 x 10^{22} Si
Atomic weight	72.60 Ge	*61.4725	*50.345	*39.2175	28.09 Si
Breakdown field (V/cm)	~10^5 Ge	$*1.5 \times 10^5$	$*2 \times 10^5$	*2.5 x 10^5	~3×10^5 Si
Crystal Structure	Diamond	Diamond	Diamond	Diamond	Diamond
Density (g/cm^3)	5.3267 Ge	*4.577	*3.827	*3.078	2.328 Si
Dielectric constant	16.0 Ge	*14.975	*13.95	*12.925	11.9 Si
Effective density of States in conduction band, N_c (cm^{-3})	1.04×10^{19} Ge				2.8×10^{19} Si
Effective density of States in valence band, N_v (cm^{-3})	6.0×10^{18} Ge				1.04×10^{19} Si
Effective Mass, m^*/m_0	Electrons	Holes	m^*_l= 1.64 m^*_t= 0.082 $m^*_{l\,h}$= 0.044 $m^*_{h\,h}$= 0.28 Ge		m^*_l= 0.98 m^*_t= 0.19 $m^*_{l\,h}$= 0.16 $m^*_{h\,h}$= 0.49 Si
Electron affinity χ(V)	4.0 Ge	*4.0125	*4.025	*4.0375	4.05 Si
Minimum Indirect Energy Gap (eV) at 300K			0.66 Ge	***0.804	*** 0.945
	***1.05	1.12 Si			
Minimum Direct Energy Gap (eV)	.7 Ge	1.6	2.5	3.1	3.4 Si
Intrinsic carrier concentration (cm^{-3})	2.4×10^{13} Ge	$*1.8 \times 10^{13}$	$*1.2 \times 10^{13}$	*0.6	

x 10^{13}	1.45 x 10^{10} Si				
Intrinsic Debye length	(μm)	0.68 Ge	*6.51	*12.34	*
18.17	24 Si				
Intrinsic resistivity	(Ω-cm)	47 Ge	*.575 x 10^5	*1.15 x 10^5	*
1.725 x 10^5	2.3 x 10^5 Si				
Lattice Constant (A)	***5.6575 Ge	***5.5960	***5.5373	***5.4825	***
5.4310 Si					
Linear coefficient of thermal expansion,		$\Delta L/L\Delta T$ (⊕C^{-1})	5.8 x 10^{-6} Ge	*5.0 x 10^{-6}	*4.2
x 10^{-6}	*3.4 x 10^{-6}	2.6 x 10^{-6} Si			
Melting point (⊕C)	937 Ge	*1056.5	*1176	*1295.5	
	1415 Si				
Minority carrier lifetime (s)		10^{-3} Ge	*1.375 x 10^{-3}	*1.75 x 10^{-3}	*
2.125 x 10^{-3}	2.5 x 10^{-3} Si				
Mobility (drift) (cm^2/V-s)		3900(electron) 1900(hole) Ge		*3300(electron)	*
1537.5(hole)	*7700(electron) *1175(hole)		*2100(electron) *812.5(hole)		
	1500(electron) 450(hole) Si				
Optical - phonon energy (eV)		0.037 Ge			
	0.063 Si				
Phonon mean free path	λ_0(Å)	105 Ge			
	76 (electron) 55 (hole) Si				
Specific heat (J/g-⊕C)		0.31 Ge	*.4075	*.505	
	*.6025	0.7 Si			
Thermal conductivity at 300 K (W/cm-⊕C)			0.6 Ge	**.11	
	**.083	**.085	1.5 Si		
Thermal diffusivity (cm^2/s)		0.36 Ge	*0.495	*.63	
	*.765	0.9 Si			
Vapor pressure (Pa)	1 at 1330⊕C 10^{-6} at 760⊕C Ge		1 at *1410⊕C 10^{-6} at *795		1 at
*1490⊕C 10^{-6} at *830⊕C		1 at *1570⊕C 10^{-6} at *865⊕C		1 at 1650⊕C 10^{-6}	
at 900⊕C Si					

* value was derived through linear approximation ; ** value was derived through subjective observation of graph/diagram [1]; *** value was derived through quadratic approximation

TABLE 1 lists physical properties of Si, Ge, and SiGe [2][3]

The linear approximations were calculated using the following function where C_{Si} represents the Silicon value, C_{Ge} represents the Germanium value, and x represents the fractional composition of Germanium:

$$a(x) = C_{Si}(1-x) + C_{Ge}(x).$$

All values in the above table for SiGe are %atm values. The values for the thermal conductivity were taken from a graph[1][7]. The values for the minimum indirect energy gap were determined from both a graph[1][8] and also from the following quadratic expression where x represents the fractional composition of Germanium:

$$E_g(x) = (1.155 - 0.43x + 0.0206x^2)\text{eV for} \quad 0 < x < 0.85 \quad [1][5]$$

EXHIBIT C

(Figure 20 of US Patent No. 6,559,494)

FIG.20

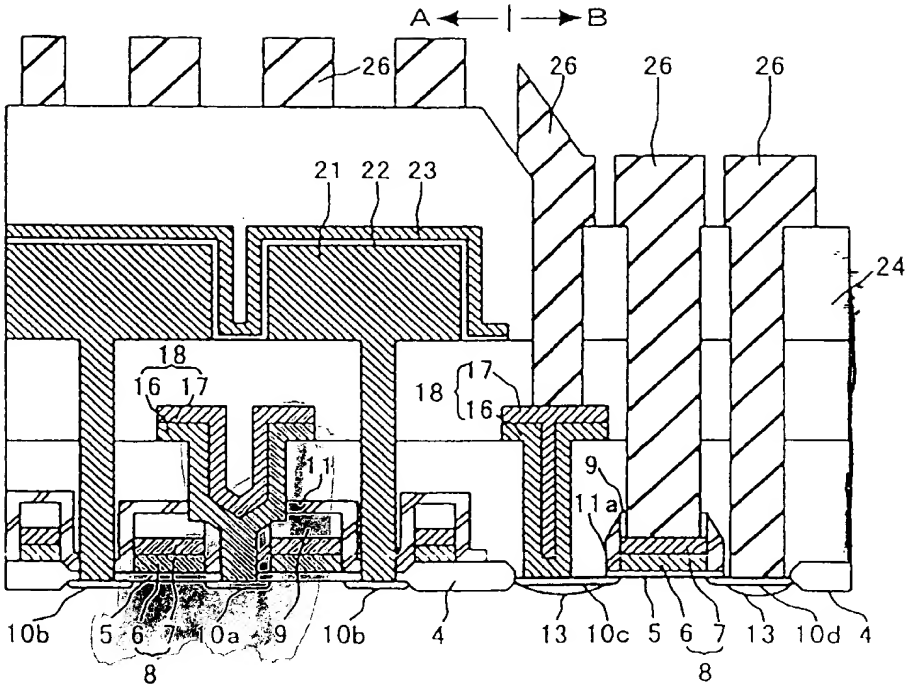

EXHIBIT C

EXHIBIT D

(Figure 6.0 of Present Invention, Serial No. 09/607,675)

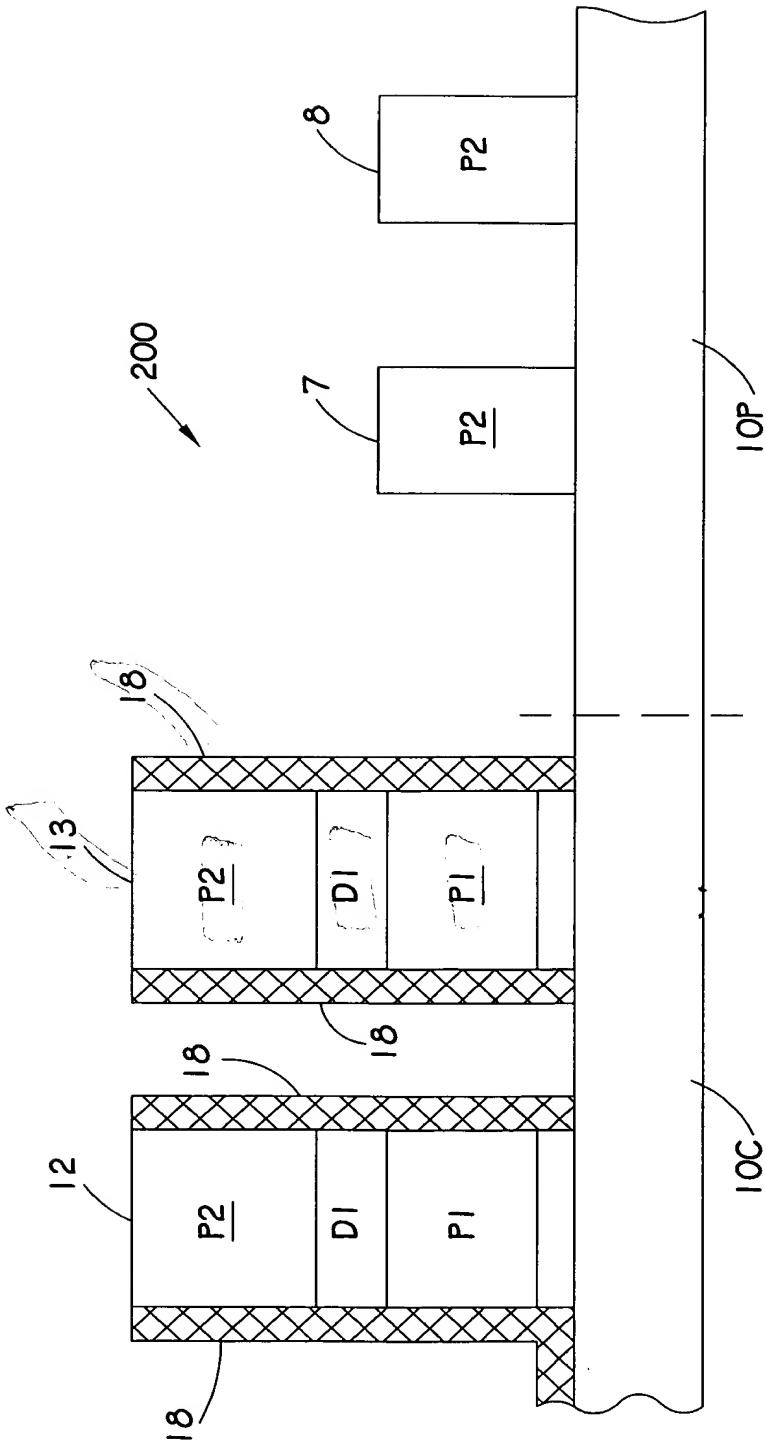

Figure 6.0

EXHIBIT D

EXHIBIT E

(Definition of "Polycrystalline Silicon, Poly Si")

Semiconductor Glossary

Semiconductor OneSource

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Term (Index)	Definition
oxygen in silicon	in moderate concentration (below 1017 cm2) oxygen may improve mechanical properties of a silicon wafer; excess oxygen may precipitate in silicon forming electrically active centers.

Term (Index)	Definition
polycrystalline silicon, poly Si	crystalline Si in which long range order is maintained only within limited grains; heavily doped poly Si is commonly used as a gate contact in silicon MOS and CMOS devices; as a cheaper than single-crystal form of silicon also used to fabricate thin film transistors and solar cells.
single-crystal material	atoms arranged following specific pattern throughout the entire piece of material; i.e., long-range order exists throughout.

Term (Index)	Definition
silicon carbide, SiC	

EXHIBIT E

EXHIBIT F

(Figure 8A of US Patent No. 6,027,971)

FIG. 8A

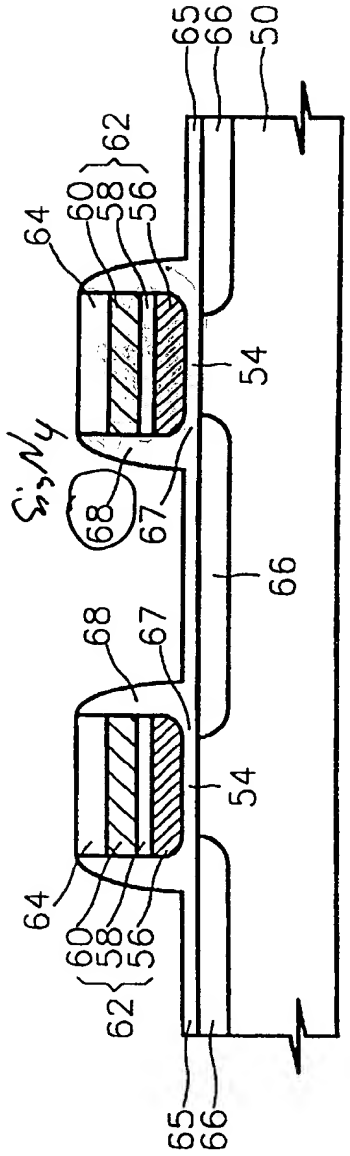

FIG. 8B

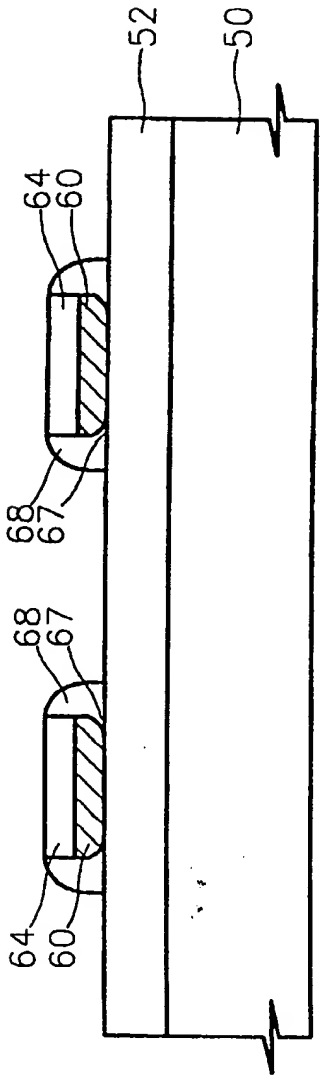

EXHIBIT F

EXHIBIT G

(Figure 10A of US Patent No. 6,027,971)

FIG. 10A

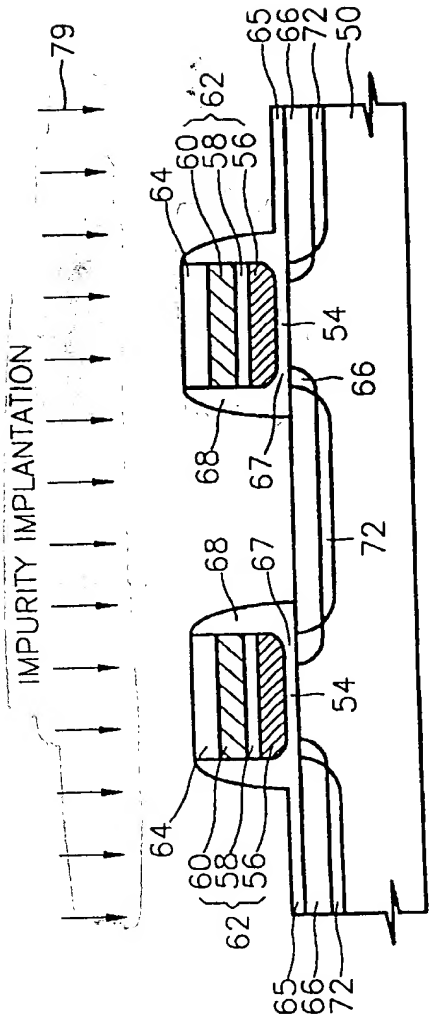

FIG. 10B

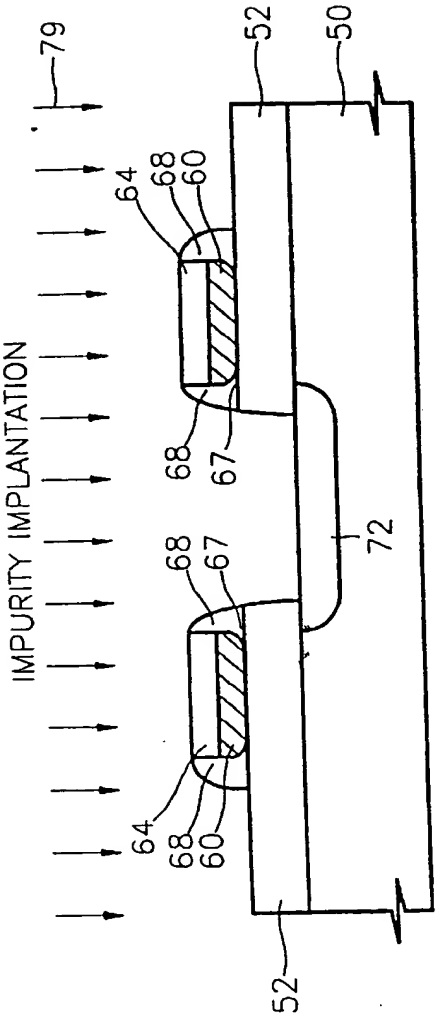

EXHIBIT G